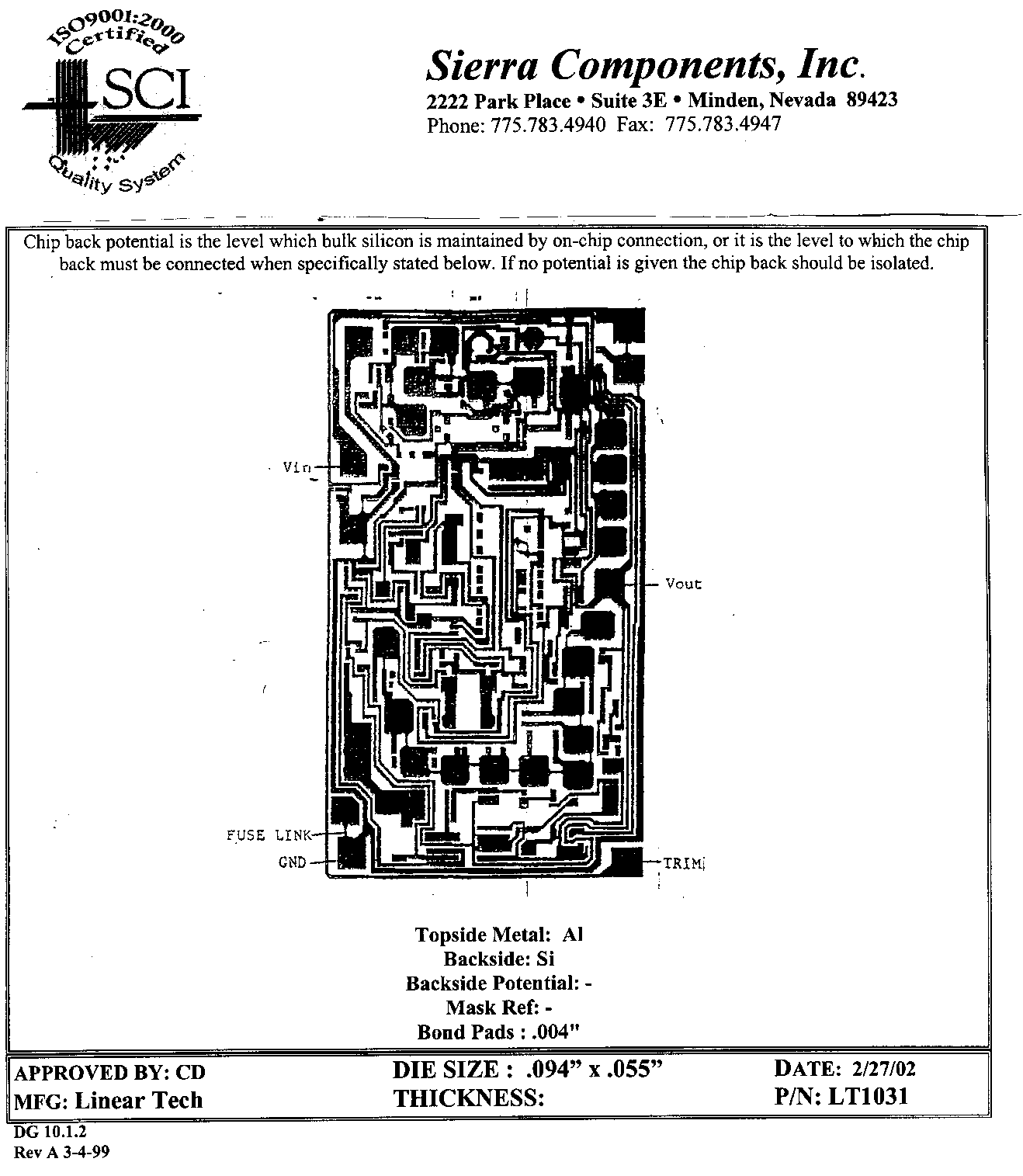
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.055”**

**PAD FUNCTION:**

1. **N/C**
2. **VIN**
3. **N/C**
4. **GND**
5. **TRIM**
6. **VOUT**
7. **N/C**



**.094”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .055” X .094” DATE: 8/21/19**

**MFG: LINEAR TECH THICKNESS .009” P/N: LT1031**

**DG 10.1.2**

#### Rev B, 7/1